PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Malcolm Betts et al	Attorney Docket No. 9-13528-156US
Serial No: 09/992,410	Group Art Unit: 2616
Filed: November 26, 2001	Examiner: Anthony M. SOL

For: Cross-Connection Of High Bandwidth Signal Traffic Across Independent Parallel Shelves

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United States Patent and Trademark Office
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U.S.A.

Sir:

Request for Pre-Appeal Review

Pursuant to 37 C.F.R. § 1.191, the Applicant has submitted a Notice of Appeal from the Examiner to the Board of Patent Appeals and Interferences, along with a Pre-Appeal Brief Request for Review. Specifically, the Applicant takes appeal from the Examiner's rejection of claims 1-2, and 4-24 under 35 U.S.C. §102(e) and/or §103(a). The Notice of Appeal has been filed in response to the Examiner's Final Action mailed March 22, 2006, and subsequent Advisory Action mailed June 6, 2006. In support of the above-noted Pre Appeal Brief Request for Review, the Applicant now submits the following arguments:

Applicant believes that the present request for Pre-Appeal Brief Review is appropriate, because of clear factual deficiencies in the rejections of record. More specifically, the Examiner's claim rejections are based on alleged teachings of the prior art, and conjecture regarding how the teaching of the cited reference might be modified, none of which are supported by the cited reference.

The Examiner's rejection

In the Examiner's Final Action mailed March 22, 2006, the Examiner asserts (at page 3):

> "Bobin discloses that switching circuits can be configured independently (Independent pointer processing)(pg.4, para 67, lines 1-2). Bobin shows in FIG. 4 10Gbit/second signal 401 that feeds into a slicer 402, which divides input signal 401 into four 2.5 Gbit/second signals/slices (STS concatenation) that feed into switching circuits 404-407 (pg. 3, para. 50, lines 4-7). Bobin further discloses that if there is a small skew in path delay across the four lanes as they are received at the splicer, a special circuitry synchronizes traffic on the four lanes to eliminate the skew (successful pointer processing) by queuing and inserting special "synchronization characters" (pg. 3, para. 60, lines 1-9; claim – modifying at least one sub-stream to emulate a conventional STS concatenation with sufficient accuracy to enable successful pointer processing through the shelf)."

These arguments are supplemented in box 11 of the Advisory action mailed June 6, 2006 as follows:

> Bobin discloses that a cross-bar switch is just one embodiment of his invention and that other embodiments, such as those supporting standard SONET transfer rates including STS-1; C-3; OC-12; OC-48; OC-192 etc., are possible (para 18). And since SONET standard supports pointer processing, the limitation of "modifying at least one sub-stream to emulate a conventional STS concatenation with sufficient accuracy to enable successful pointer processing through the shelf" in claims 1 and similarly in claim 17, is taught by Bobin. It is noted that the Examiner interprets the phrase "with sufficient accuracy" broadly since there is no indication of what constitutes "sufficient" other than "to enable successful pointer processing". Again, "successful" is interpreted broadly since what is considered "successful" is subjective. [underlining added]

As noted in Applicant's response filed May 18, 2006, the person of ordinary skill in the art will instantly recognise that none or these assertions, particularly as they relate to the very well known SONET standard, are supported by the teaching of Bobin.

United States Patent Application Publication No. 2003/0002779 (Bobin)

United States Patent Application Publication No. 2003/0002779 (Bobin) teaches a system for switching signals between optical fibers. Upon receiving a plurality of optical input signals, the system divides each of the optical input signals into N input slices, wherein each input slice carries 1/Nth of the data for a given input signal. Next, the system distributes the N input slices to N switching circuits. This allows the N input slices to be switched in parallel to N corresponding output slices. Next, the system forms a plurality of optical output signals, wherein a given optical output signal is formed by receiving N output slices from the N switching circuits, and splicing the N output slices together to form the given optical output signal. [Abstract]

According to Bobin, each of the N switching circuits may be provided by a cross-bar switch (Para. 38, lines 4-6), and may be independently configured (Para 67). Skew between each of the N slices traversing the N switching circuits between the slicer and the splicer may be compensated by queing in the splicer, and inserting synchronization characters in each slice (Para. 60)

At Para. 18, Bobin states that "each optical input signal supports at least one of the standard Synchronous Optical Network (SONET) transfer rates …" The Examiner appears to assert that this one-sentence constitutes a teaching of modifying of Bobin's switch fabric to replace the cross-bar switches with "two or more parallel shelves of a switch core of the cross-connect, wherein each shelf has a respective independent pointer processing state machine" as required by the present claims. Such an extrapolation is entirely unsupported, and is clearly not valid. The person of ordinary skill in the art will instantly recognise that whether or not the input optical signal (e.g. 401 of Bobin FIG. 4) supports SONET transfer rates implies exactly nothing about the switching circuits (e.g. 404-407) within the switch fabric. Cross-bar switches can easily support SONET transfer rates. Similarly, the person of ordinary skill in the art will recognise that a one-sentence reference to independently configured switch elements (e.g. at para 67), does not in any way imply the provision of independent pointer processing state

machines. Bobin is silent with respect to pointer processing. Furthermore, absent the teaching of the present invention, the person of ordinary skill in the art will recognise that the Examiner's proposed modification is inoperative, for at least the reasons described in detail in the Background to the present invention.

Apparently undeterred by these difficulties, the Examiner further appears to assert that the above-noted two sentences also constitute a teaching of modifying at least one substream to emulate an STS concatenation. Again such extrapolation is utterly unfounded. Bobin does not mention STS concatenations, and does not mention modifying substreams to emulate any particular signal format, much less an STS concatenation. Bobin does teach inserting synchronization characters, but to suggest that the mere insertion of synchronization characters is in any way equivalent to emulating an STS concatenation (or somehow accomplishes the same result) is absurd. In fact, the one and only source for a teaching of modifying a substream to emulate an STS concatenation (and the motivations for doing so) is the Applicant's own disclosure.

With particular reference to "successful pointer processing" being a subjective judgement, thereby enabling a broad interpretation of the claimed feature of "modifying at least one substream to emulate an STS concatenation", the skilled artisan will recognise that there absolutely nothing subjective about whether or not pointer processing is "successful". As is very well known in the art, a conventional SONET pointer processor state machine detects various errors in the signal and the pointer processing operation. The SONET standard also defines certain performance criteria, such as latency and bit error rate, which must be maintained. Obviously, "successful" pointer processing necessarily means, at the very least, that the pointer processor state machine does not trigger (or enter) an error state while processing the signal. The person of ordinary skill in the art will recognise that there is absolutely nothing subjective about whether or not an error state is triggered, as the various criteria are all fully defined in the SONET standard.

In light of the foregoing, it is submitted that the Examiner's claim rejections are entirely lacking proper factual basis, wherefore Pre-Appeal panel review of this case is believed to be appropriate, and early action in that respect is courteously solicited.

If any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this response, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 19-5113.

Respectfully submitted,
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